



A WIDE-RANGE PLL USING SELF HEALING PRESCALER/VCO IN A 65 NM CMOS

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Abstract: The variability and leakage current in nanoscale CMOS technology may degrade the circuit performances significantly. To accommodate the above issues in a wide range phase-locked loop (PLL), a self-healing prescaler, a self-healing voltage-controlled oscillator (VCO), and a calibrated charge pump (CP) are presented. This PLL is fabricated in a 65-nm CMOS technology and its active area is 0.0182 mm. For the self-healing VCO, its measured frequency range is from 60 to 1489MHz. When this PLL operates at 855MHz, the measured Rms and peak-to-peak jitters are 8.03 and 55.6ps respectively. This PLL consumes 4.3mW from 1.2V supply without buffers. The proposed provides several techniques to avoid the circuits to degrade by the process variability and leakage current in nanoscale CMOS technology. In addition, the active area and power of this PLL will be increased because of these self-healing circuits. To reduce the active area, a state look ahead logic is used for counting in order to reduce the area of counter. A high speed wide-range parallel counter that achieves high operating frequencies through a novel pipeline partitioning methodology (a counting path and state look-ahead path), using only three simple repeated CMOS-logic module types: an initial module generates anticipated counting states for higher significant bit modules through the state look-ahead path, simple D- flip-flops and 2-bit counters. The state look-ahead path prepares the counting path's next counter state prior to the clock edge such that the clock edge triggers all modules simultaneously, thus concurrently updating the count state with a uniform delay at all counting path modules/stages with respect to the clock edge. The structure is scalable to arbitrary N-bit counter widths (2-to-N range) using only the three module types and no fan-in or fan-out increase. The counter's delay is comprised of the initial module access time, one three-input AND-gate delay and a D-flip-flop setup-hold time. The counter uses a 0.15 μm^2 TSMC digital cell library and verified maximum operating speeds of 2 and 1.8 GHz for 8 and 17-bit counters, respectively. Finally, the area of a sample 8-bit counter was 78 125 μm^2 (510 transistors) and consumed 13.89mW at 2 GHz.

Index Terms - Leakage current, nanoscale CMOS technology, phased-locked loop (PLL). Architecture design, high-performance counter design, parallel counter design, pipeline counter design

I.INTRODUCTION

When a CMOS technology approaches to a nanometer scale, the non-idealities such as variability and leakage current, may significantly affect the circuit performances. The process variability leads to the large variations to degrade the device matching and performances. It may result in only a few dies on a wafer to meet the target performance specifications. The undesired leakage currents also degrade the accuracy and resolution of analog circuits and make digital dynamic circuits not to work properly. A phase-locked loop (PLL) is widely employed in wire line and wireless communication systems. The poor device matching and leakage current vary the common-mode voltage of a ring-based voltage-controlled oscillator (VCO) over an it's wide frequency range. It may limit the oscillation frequency range of a VCO and causes a VCO not to oscillate in a worst case. To realize a wide-range PLL, the divider following a VCO should operate between the highest and lowest frequencies. When a PLL works at a higher frequency which the static circuits cannot operate, dynamic circuits are needed. To deal with the process variability and leakage current in nanoscale CMOS process, a self-healing prescaler, a self-healing VCO and a calibrated charge pump are used. In addition, the active area and power of this PLL will be increased because of these self-healing circuits. To reduce the active area, a state look ahead logic is used for counting in order to reduce the area of counter.

II.CIRCUIT DESCRIPTION

A. Phase-Locked Loop

The PLL is composed of a phase-frequency detector (PFD), a digital-controlled CP, a lock detector (LD), a time-to-digital converter (TDC) with a 4-bit encoder, a self-healing VCO, a programmable divider, and a second-order passive loop filter. The programmable divider is composed of a 5-bit counter, a 3-bit swallow counter, a modulus control, and a self-healing divide-by-4/5 prescaler. When this PLL locks, the LD is enabled to turn on the TDC and an encoder. A 4-bit TDC digitizes this static phase error to reflect the amount of the current mismatching. Then, the digital code of this TDC is used to calibrate the charge pump. To deal with the process variability and leakage current in nanoscale CMOS process, a self-healing prescaler, a self-healing VCO, and a calibrated CP are presented. Due to additional active devices, the jitter performance of a self-healing PLL will be degraded, compared to a PLL without a self-healing technique. In addition, the active area and power of this PLL will be increased because of these self-healing circuits.

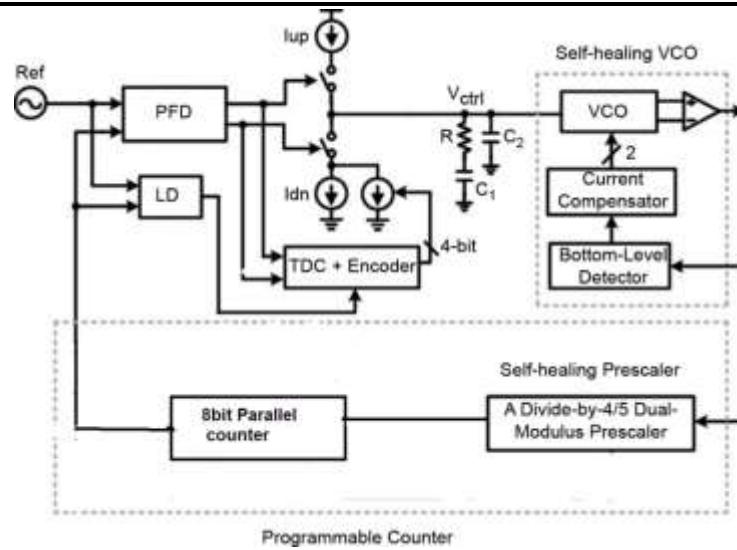


Fig.1. Proposed PLL



B. Parallel counter

To reduce the active area, a state look ahead logic is used for counting in order to reduce the area of counter. Counters are widely considered as essential building blocks for a variety of circuit operations such as programmable frequency dividers, shifters, code generators, memory select management, and various arithmetic operations. Since many applications are comprised of these fundamental operations, much research focuses on efficient counter architecture design. Counter architecture design methodologies explore tradeoffs between operating frequency, power consumption, area requirements, and target application specialization. Early design methodologies improved counter operating frequency by partitioning large counters into multiple smaller counting modules, such that modules of higher significance (containing higher significant bits) were enabled when all bits in all modules of lower significance (containing lower significant bits) saturate. Initializations and propagation delays such as register load time, AND logic chain decoding, and the half incrementer component delays in half adders dictated operating frequency. Subsequent methodologies improved counter operating frequency using half adders in the parallel counting modules that enabled carry signals generated at counting modules of lower significance to serve as the count enable for counting modules of higher significance, essentially implementing a carry chain from modules of lower significance to modules of higher significance.

The carry chain cascaded synchronously through intermediate D-type flip-flops (DFFs). The maximum operating frequency was limited by the half adder module delay, DFF access time, and the detector logic delay. Since the module outputs did not directly represent count state, the detector logic further decoded the module outputs to the outputted count state value. Further enhancements improved operating frequency using multiple parallel counting modules separated by DFFs in a pipelined structure. The counting modules were composed of an incrementer that was based on a carry-ripple adder with one input hardcoded to "1". In this design, counting modules of higher significance contained more cascaded carry-ripple adders than counting modules of lower significance. Each counting module's count enable signal was the logical AND of the carry signals from all the previous counting modules (all counting modules of lower significance), thus prescaling clocked modules of higher significance using a low frequency signal derived from modules of lower significance. Due to this prescaling architecture, the maximum operating frequency was limited by the incrementer, DFF access time, and the AND gate delay. The AND gate delay could potentially be large for large sized counters due to large fan-in and fan-out parasitic components. Design modifications Enhanced AND gate delay, and subsequently operating frequency, by redistributing the AND gates to a smaller fan-in and fan-out layout separated by latches. However, the drawback of this redistribution was increased count latency (number of clock cycles required before the output of the first count value). In addition, due to the design structure, this counter architecture inherited an irregular VLSI layout structure and resulted in a large area overhead. The carry look-ahead circuit used a prescaler technique with systolic 4-bit counter modules [which used T-type flip-flops (TFFs)], with the cost of an extra detector

circuit. The detector circuit detected the assertion of lower order bits to enable counting in the higher order bits. To further improve operating frequency, Kakarountas's design used DFFs between systolic counter modules. The clock period was bounded by the delay of two input gates in addition to the TFF access and setup-hold time. Large counter widths incurred an additional three input logic gate delay. However, since the

counter design was limited by control signal broadcasting, Kakarountas's design was not practical for large counter widths even though the Xilinx Data Book shows that several counter designs with the highest operating frequencies use prescaler techniques. In order to create a more efficient architecture for large counter widths and more amenability to a wider application range, counter architectures, such as up/down counters, added extra(redundant) registers (while still using partitioned counter modules to store the previous counter state during a counter state transition (counter increment). Thus, when the counting direction changed (from up to down or down to up), the contents of these count state registers determine the next counter state.

C. Parallel Counter Architecture

- 1) A single clock input triggers all counting modules simultaneously, resulting in an operating frequency independent of counter width (assuming ideal parasitic capacitance on the clock wire path, without loss of generality). The total critical path delay (regardless of counter width) is uniform at all counting stages and is equal to the combination of the access time of a 2-bit counting module, a single three-input AND gate delay, and the DFF setup-hold time.
- 2) Our parallel counter architecture leverages modularity, which enables high flexibility and reusability, and thus enables short design time for wide counter applications. The architecture is composed of three basic module types separated by DFFs in a pipelined organization. These three module types are placed in a highly repetitious structure in both the counting path and the state look-ahead paths, which limits localized connections to only three signals
- 3) The counter output is in radix-2 representation so the count value can be read on-the-fly with no additional logic decoding.
- 4) Unlike previous parallel counter designs that have count latencies of two or three cycles, depending on the counter width, our parallel counter has no count latency, which counter as a single mode counter, which sequences through a fixed set of preassigned count states, of which each next count state represents the next counter value in sequence. The counter is partitioned into uniform 2-bit synchronous up counting modules. Next state transitions in counting modules of higher significance are enabled on the clock cycle preceding the state enables the count value to be read on-the-fly. Transition using stimulus from the state look-ahead path. Therefore, all counting modules concurrently transition to their next states at the rising clock edge (CLKIN). In this section, we describe the architecture and functionality of our parallel counter, the derivation of each counter state equation, and area analysis.

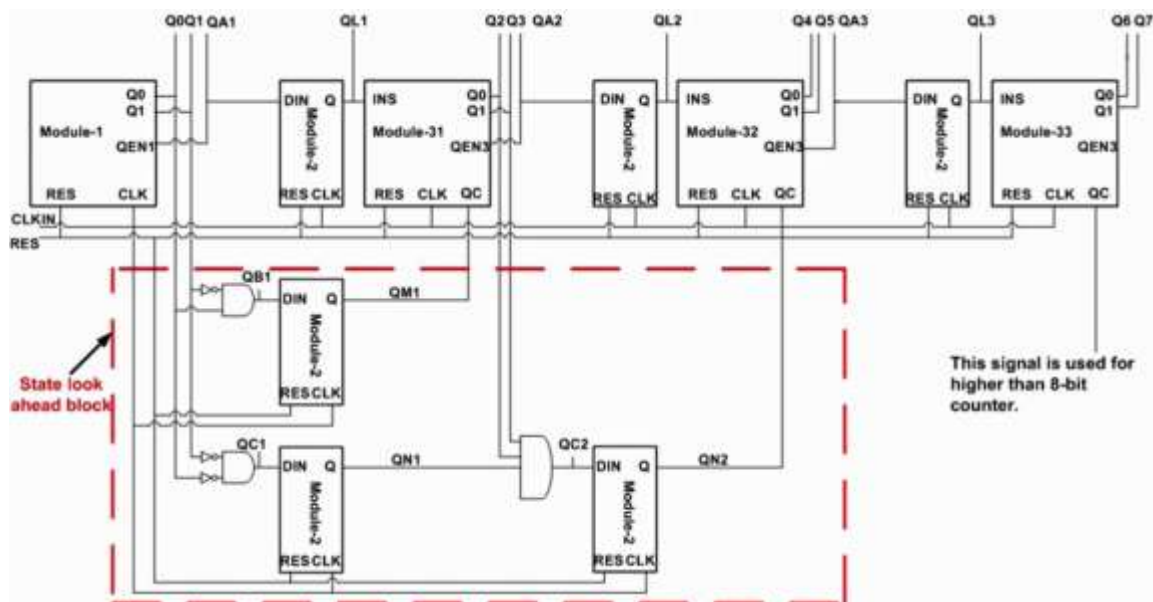
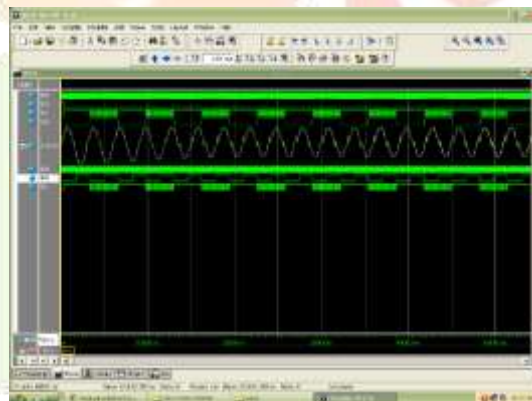


Fig.2 Functional block diagram of parallel counter

III.SIMULATED RESULTS



D.Architectural Functionality

The counting path's counting logic controls counting operations and the state look-ahead path's state look-ahead logic anticipates future states and thus prepares the counting path for these future states. Fig. 1 shows the three module types Fig. 2. Module-1 (a) hardware schematic and (b) state diagram. Module-1 and module-3 are exclusive to the counting path and each module represents two counter bits. Module-2 is a conventional positive edge triggered DFF and is present in both paths. In the counting path, each module-3 is preceded by an associated module-2. Module-3's serves two main purposes. Their first purpose is to generate all counter bits associated with their ordered position and the second purpose is to enable (in conjunction with stimulus from the state look-ahead path) future states in subsequent module-3's (higher values) in conjunction with stimulus from the state look-ahead path. Thus, instead of the modules of higher significance requiring the AND of all enable signals from modules of lower significance, modules of

higher significance are simply enabled by the module-3 preceding module-2. 1) *Counting Path*: Module-1 is a standard parallel synchronous binary 2-bit counter, which is responsible for low-order bit counting and generating future states for all module-3 in the counting path by pipelining the enable for these future states through the state look-ahead path. Fig. 2 depicts the (a) hardware schematic and (b) state diagram for module-1. Module-1 outputs (the counter's two low-order bits) and (the 1 in denotes that this is the for module-1). Connects to the module-2's input. The placement of module-2s in the counting path is critical to the novelty of our counter structure. Module-2s in the counting path act as a pipeline between the module-1 and module-3 1 and between subsequent module- s. Module-2 placement increases counter operating frequency by eliminating the lengthy AND-gate rippling and large AND gate fan-in and fan-out typically present in large width parallel counters.

IV. CONCLUSION

To deal with the process variability and leakage current in nanoscale CMOS process, a self-healing prescaler, a self-healing VCO, and a calibrated CP are presented. In addition, the active area and power of this PLL will be increased because of these self-healing circuits. To reduce the active area, a state look ahead logic is used for counting in order to reduce the area of counter. A high speed wide-range parallel counter that achieves high operating frequencies through a novel pipeline partitioning methodology (a counting path and state look-ahead path), using only three simple repeated CMOS-logic module types thus reducing the area of the counter.

V. REFERENCES

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