



A Novel Design Of An Inductor-Less Mm-Wave DIQ Generator For 5G Applications

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Abstract: This paper introduces a new design of inductor-less DIQ generator optimized for millimeter-wave (mm-wave) applications of 5G. Conventional DIQ generators are based on bulky inductors, which make these circuits quite big and complex, while the proposed design exploits an inductor-free, compact architecture to provide more efficient and scalable solutions for integration into modern communication systems. Taking advantage of advanced techniques in semiconductor fabrication, the DIQ generator has 5G high frequency with high phase accuracy and low power consumption, as are now demanded by modern wireless communication. Simulations and experimental results show the efficacy of the approach with improved bandwidth, phase noise, and overall efficiency. This inductor-less DIQ generator opens up a pathway for more compact and power-efficient components of the next generation wireless technology.

Index Terms - 5G Communications, Millimeter-wave(mm-wave) circuits, Phase Shifters, Differential Amplifier, Quadrature Phase Signals, Cascoded Amplifier.

I. INTRODUCTION

In the rapidly advancing field of 5G communications, the design of compact, efficient, and high-performance millimeter-wave (mm-wave) circuits is critical. Classic architectural solutions for the DIQ generators strongly depend on inductors, these are faced with significant challenges relating to increased size, reduced integration capability, and intricate processes of fabrication.

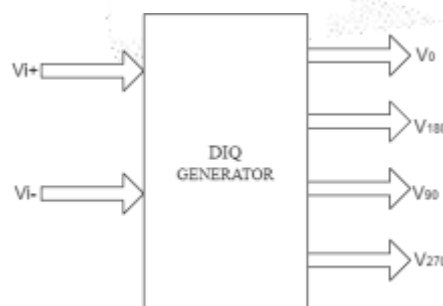


Fig. 1 Block Diagram of DIQ Generator

The Block Diagram of the DIQ Generator is shown in the Fig. 1. In which it takes the two input signals i.e. V_{i+} , V_{i-} and generates the quadrature phase signals having a phase difference of 90 degrees with each other they are V_0 , V_{90} , V_{180} , V_{270} .

A Direct In phase and Quadrature (DIQ) Generator is a circuit used to produce quadrature signals, which are having a 90-degree phase difference. Such signals are critical for very wide range of applications: phase and amplitude modulation, image rejection, and quadrature down conversion in RF receiver front-ends. In this work on the validity of DIQs for the image rejection in RF systems, it has been done with knowledge of many other applications in which circuits may require a 90-degree phase shift. Mainly DIQ Generators are divided into two types based on their size. Being the one directional coupler or design, and most commonly used in

RF applications, for phased arrays and image rejection, they have low loss and are excellently isolated from each other. Hybrid couplers and Lange couplers are commonly employed. They operate at high frequencies, but they occupy a relatively wide physical space due to the requirement of having transmission lines of $1/4$ wavelength. Some designs like Lange couplers are complicated and need many design considerations, such as the introduction of bonding wires.

Another approach involves quadrature all-pass filters using resistors, capacitors, and inductors to generate quadrature signals. This method may, however, involve larger physical implementations and offer very demanding implementation standards as in the case of millimeter-wave RF receivers. To save space, RC poly-phase filters (PPFs), exist, but come with compromises such as increased signal loss, and higher power consumption. Designs for wide-band RC PPFs produce usually 3 dB loss, which requires amplifiers to boost the signal for reaching the required strength, resulting in increased power consumption. Some designs include even hybrid designs that combine RC PPFs with transformers or hybrid couplers providing broader bandwidth and correcting I/Q mismatches; however, in this aspect, they can be larger than pure RC PPF.

II. LITERATURE SURVEY

Paper "A 15–38 GHz Vector-Summing Phase-Shifter With 360° Phase-Shifting Range Using Improved I/Q Generator" [1] throws light on the importance of phase shifters in the context of phased array communication systems, which are indispensable for beam steering. Feng quiet al. proposed methodology is vector-summing phase shifter (VSPS). The shortcomings of this paper are Capacitive Loading Effects, Complexity of Design. The paper "A Low Phase Error Vector Modulator Using TEST Tunable I/Q Generator for mm Wave Communication"[2] points out that the high demand for millimeter-wave systems impelled by developments in 5G and satellite communications owes to a big challenge while designing high performance phase shifters in the perspective of gain, phase error, phase resolution and low power consumption. Jinhyun et al. The proposed methodology from Kim is to design a tunable I/Q generator in a 28nm CMOS process, achieving a 22.5° phase shift with an average RMS phase error of 2.89°. Limitations include: Limited Bandwidth Phase Error at Higher Frequencies.

The presented contribution "An mm-Wave CMOS Active Phase Shifter with a Low-Loss I/Q Generator for 5G Applications" [3] describes a new design of a mm-wave phase shifter based on state-of-the-art CMOS technology. A method of achieving efficient phase shifts for 5G signals is proposed by Yitong Xiong et al. where a hybrid high-pass/low-pass network HHLN is used to achieve minimal signal losses. The advantage of such an HHLN is that no resistance is added into the RF path causing very low insertion losses. The disadvantage of this technique, in contrast, is that the phase shifters can only work in the limited frequency range of 35 to 43 GHz.

In [4], "A 25–30-GHz RMS Error-Minimized 360° Continuous Analog Phase Shifter Using Closed-Loop Self-Tuning I/Q Generator" discusses a novel kind of phase shifter developed to operate over a wide frequency range with minimum error at low power consumption. The proposal in the paper presented by Naina Singhal et al., is to design the self-tuning I/Q generator in such a way that it will automatically minimize the errors. Limitations of the paper: It adds extra complexity in design and consumes more power.

In the following paper "A 2–20-GHz 360° Variable Gain Phase Shifter MMIC with Reverse Slope Phase Compensation" [5] describe a 2-20-GHz vector-sum variable gain phase shifter VGPS monolithic microwave integrated circuit MMIC for ultra-broadband phased-array application [5]. The proposed approach by the authors, Yitong Xiong et al., was to develop a 2-20-GHz variable gain phase shifter using an active power splitter to generate accurate I/Q signals and then enhanced it by a reverse-slope phase compensation technique to maintain its accuracy over a broad frequency range. The limitations of this paper are that the ultra-broadband impedance matching and phase accuracy introduce relatively higher power consumption[5], yielding a larger quiescent current.

III. DESIGN OF AN INDUCTOR LESS DIQ GENERATOR

The proposed Schematic of our DIQ Generator composed of only one pair of Resistor and Capacitor and Two differential amplifiers. Actually most of the differential amplifiers are having resistors as their load. By increasing the load resistance we can increase the gain of the differential amplifier. But at the the same time ,by increasing the load resistance the voltage drop across the load resistance is also increases which is undesirable. So in our design the resistor in the differential amplifier is replaced with the current source so we can minimize the voltage drop across the resistors. An ideal current source is characterized by infinite circuit resistance. Its infinite gain enables it to serve as a common-source amplifier stage, delivering constant current irrespective of the voltage drop across it. However, it is well established that in practice, a current source has

finite but still very large resistive characteristics. This high resistance still produces a large gain, but the current it delivers does change, albeit only slightly, with applied voltages across it.

The proposed design is similar as [6] except for the addition of the PMOS transistor as a current source and in place of the current mirror we are using only one diode based current mirror. When choosing the size of a PMOS transistor, it's important to remember that its mobility is 2-3 times lower compared to an NMOS transistor. To account for this difference, the width-to-length (W/L) ratio of the PMOS should be made 1.5 to 3 times larger than that of the NMOS to ensure balanced performance.

If μ_p equal to $\left(\frac{\mu_n}{2}\right)$ then

$$I_{D,p} = \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L}\right)_p (V_{gs} - V_{th})^2 \quad (1)$$

$$= \frac{1}{2} \left(\frac{\mu_n}{2}\right) C_{ox} \left(\frac{W}{L}\right)_n (V_{gs} - V_{th})^2 \quad (2)$$

$$= I_{D,n} \quad (3)$$

requiring $\left(\frac{W}{L}\right)_p$ equal to $2 \left(\frac{W}{L}\right)_n$

When beginning the design iteration process, the size ratios of the NMOS and PMOS transistors should be set in a similar way. The PMOS transistor should be made approximately 1.5 to 3 times wider than the NMOS, assuming the length is kept constant.

In the saturation region, PMOS needs to be suitably biased in order to work well. The condition for the PMOS is that it must be:

$$|V_{ds}| \geq |V_{gs}| - |V_{th}|. \quad (4)$$

Nevertheless, in principle, neither R (resistance) nor C (capacitance) is dependable for controlling a 90-degree phase shift: the phase shift is constant across all frequencies. The work presents transitions of output signals with the same amplitude only when $\omega = 1/RC$, hence a proper choice of R and C is required. This can be expressed as:

$$\omega = 2\pi f = \frac{1}{RC} \quad (5)$$

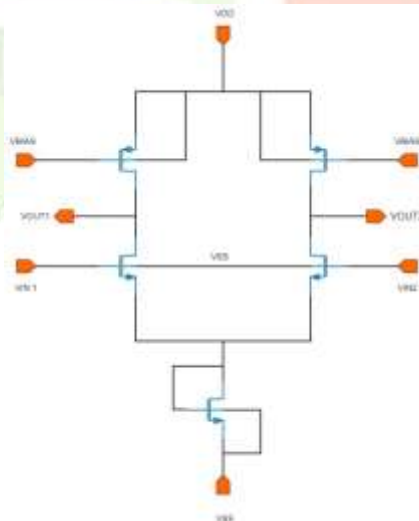


Fig.2 Schematic of the Differential amplifier

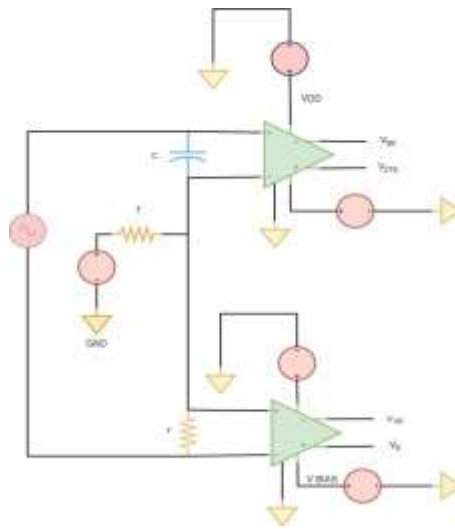


Fig.3 Test Bench Schematic for DIQ

By Using the one differential amplifier we get the phase shift of 90 and 270 degrees. For getting the phase shifts of 180 and

0 degrees we want to use two stages of differential amplifiers

Such that the two differential amplifiers connected in the cascoded form as shown in the Fig 3. Our DIQ generator consists of two Stages. First Stage is RC Network and the Second stage is the differential amplifiers. The voltage across the Capacitor and the Resistor is fed to the differential amplifiers. By voltage division rule the voltage across the capacitor and the resistor is given by the

$$V_C = \left(\frac{1}{1+SRC} \right) * V_i \quad (5)$$

Similarly

$$V_R = \left(\frac{SRC}{1+SRC} \right) * V_i \quad (6)$$

The Two differential amplifiers sample the two voltage signals, resulting in quadrature output voltages at $0^\circ, 90^\circ, 180^\circ$, and 270° . Specifically, the relationship between the outputs is given by

$$\frac{V_{90^\circ}}{V_{0^\circ}} = -\frac{1}{SRC} \quad (7)$$

Where the negative sign comes from the gain of the differential amplifier indicating the output waveform at V_{90° will lag behind the one at V_{0° .

IV. RESULTS AND DISCUSSION

The Schematic which is shown in the Fig.2 is implemented in the cadence software and achieved the phase shifts of 90° and 270° . For getting the 180° and 0° the overall schematic which is shown in the Fig.3 is implemented and the output is shown in the Fig.4 and also the power is calculated and we are getting 0.227mW which is very low power when compared to [6]. The power consumption of the different QPGs are compared in the following table with our proposed design. The simulation of the total DC power analysis is shown in the Fig 9. Then S parameters are also calculated which is shown in the Fig 5, Fig 6, Fig 7, Fig 8. By doing S11 parameter calculation we get a bandwidth of 224 GHz and getting a gain of -763.498mdB.

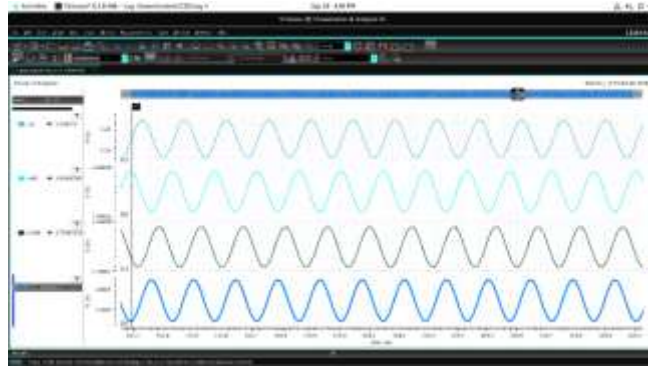


Fig.4 Output wave forms of the Proposed Circuit

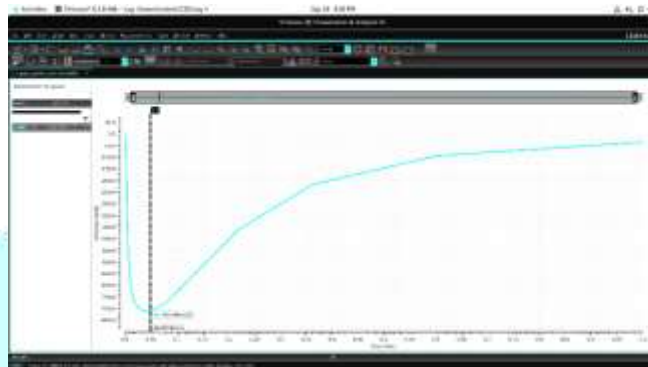


Fig.5 Simulation of S11 parameter analysis

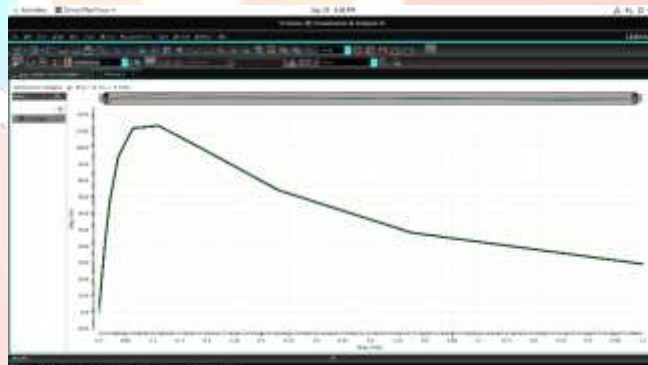


Fig.6. Simulation of S12 parameter

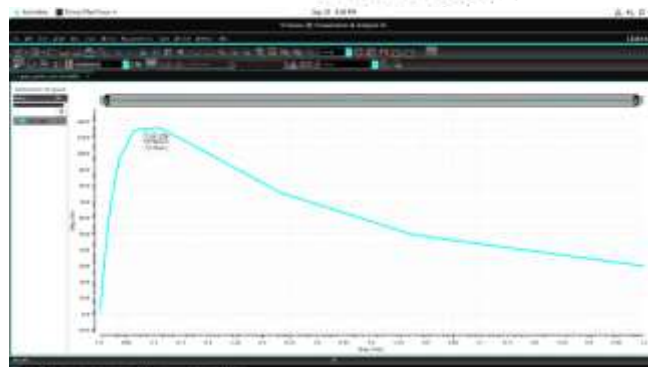


Fig.7 Simulation of S21 Parameter analysis

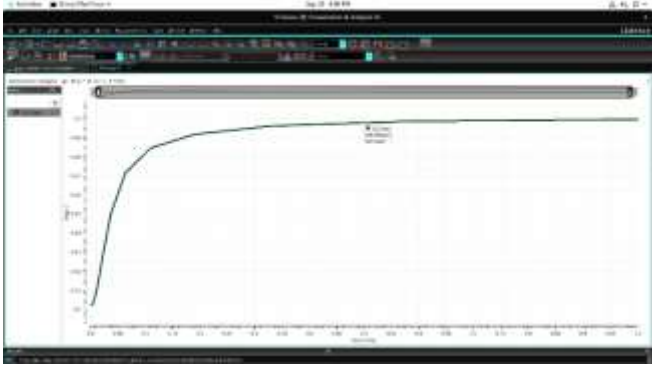


Fig.8 Simulation of S22 parameter Analysis

Our design is purely Inductor less design when compared to the [1-4].In[1]they get a power of 19.2 mw and [2] has power consumption of 28.2 mw, similarly for [3],[4] has power consumption of 17.3mW,11.2mw.The Total DC power calculation is shown in the Fig.9.



Fig.9 Simulation of DC power Analysis

Table 4.1: TECHNOLOGY AND POWER COMPARISION

Reference	Qiu , et al 2021 [1]	Kim, et al 2023 [2]	Yitong, et al. 2021 [3]	Singhal ,et al 2022 [4]	Proposed work
Technology	CMOS-65nm	CMOS-28nm	CMOS-90nm	CMOS-65nm	CMOS-180nm
Power (mW)	1.2	2.8	1.3	1.2	0.227
No of Inductors	4	3	6	8	0
Frequency (GHz)	15-38	31-36	35-43	25-30	210-260
No of Transistors	0	0	5	9	10

V. CONCLUSION

In this work, we proposed a novel inductor-less mm-wave direct in-phase and quadrature (DIQ) generator tailored to 5G applications. In such design, the necessity to introduce large inductors results in problems like increasing chip area and limited flexibility in integration. The proposed above DIQ generator of excellent phase accuracy, in conjunction with amplitude balance and low power, is rendered with the aid of modern circuit techniques. Simulation results confirm that it will be able to work efficiently in the mm-wave frequency range, which is quite stringent for 5G communication systems.

Compact, inductor-less design makes it very useful for future modern RFICs where size, power, and performance are paramount. In that context, it reduces the overall footprint while streamlining the manufacturing process, presenting a very promising direction for the application of future high-frequency wireless communications systems. Further developments in that line may be considering optimizations to improve its robustness so that it can be used for other emerging wireless standards beyond 5G.

REFERENCES

- [1] Qiu, Feng, et al. "A 15–38 GHz vector-summing phase-shifter with 360° phase-shifting range using improved I/Q generator." *IEEE Transactions on Circuits and Systems II: Express Briefs* 68.10 (2021): 3199-3203
- [2] Kim, Jinhyun, Seongwoog Oh, and Jungsuek Oh. "A low phase error vector modulator using TEST tunable I/Q generator for mmWave communication." *IEEE Microwave and Wireless Technology Letters* 33.7 (2023): 1055-1058.
- [3] Xiong, Yitong, et al. "An mm-wave CMOS Active Phase Shifter with a Low-Loss I/Q Generator for 5G Applications." *2021 IEEE 4th International Conference on Electronics and Communication Engineering (ICECE)*. IEEE, 2021
- [4] Singhal, Naina, and SM Rezaul Hasan. "A 25–30-GHz RMS error-minimized 360° continuous analog phase shifter using closed-loop self-tuning I/Q generator." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 30.6 (2022): 720-731.
- [5] Y. Xiong, Y. Pu, Z. Yu, Y. Yao, X. Huang and G. Wang, "A 2–20-GHz 360° Variable Gain Phase Shifter MMIC With Reverse-Slope Phase Compensation," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 12, pp. 5180-5193, Dec. 2023, doi: 10.1109/TCSI.2023.3319967.
- [6] Zhou, Xue Ru. *A Novel Inductorless Low-Powered Quadrature Phase Generator for High-Frequency Communications*. MS thesis. The Cooper Union for the Advancement of Science and Art, 2024.
- [7] Cheng, Guoxiao, et al. "CMOS variable-gain phase shifter based on time-varying vector-sum method and its application to Ku-band phased array." *Microelectronics Journal* 131 (2023): 105672.
- [8] Hoznian, Hamed, and Amir Nikpaik. "A wideband and low-power mm-wave variable-gain phase shifter based on a source-switching scheme." *AEU-International Journal of Electronics and Communications* 177 (2024): 155230.
- [9] Ahamed, Raju, et al. "A 200–250-GHz phase shifter utilizing a compact and wideband differential quadrature coupler." *IEEE Microwave and Wireless Components Letters* 32.7 (2022): 883-886.
- [10] Li, Xuguang, et al. "A 30–36 GHz passive hybrid phase shifter with a transformer-based high-resolution reflect-type phase shifting technique." *IEEE Transactions on Circuits and Systems II: Express Briefs* 68.7 (2021): 2419-2423.
- [11] Wu, Tianjun, et al. "A 51.5-64.5 GHz active phase shifter using linear phase control technique with 1.4 phase resolution in 65-nm CMOS." *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. IEEE, 2019.
- [12] Dong, Zhipeng, et al. "A CMOS 10-20 GHz Full 360° Phase Shifter with 11 dB gain using RLC Load Quadrature Signal Generator." *2021 International Conference on Microwave and Millimeter Wave Technology (ICMMT)*. IEEE, 2021.
- [13] Chen, Zipeng, Haikun Jia, and Baoyong Chi. "A 27–31 GHz 6-bit phase shifter with low phase error/gain variation in 65 nm CMOS." *Microelectronics Journal* 104 (2020): 104906.
- [14] Cusmai, Marco, et al. "A 0.92-pJ/b PAM-4 and 0.61-pJ/b PAM-6 224-Gb/s DAC-Based Transmitter in 3-nm FinFET." *IEEE Journal of Solid-State Circuits* (2024).
- [15] Jung, Minjae, and Byung-Wook Min. "A compact Ka-band 4-bit phase shifter with low group delay deviation." *IEEE Microwave and Wireless Components Letters* 30.4 (2020): 414-416.

- [16] Li, Zhennan, Zhiqun Li, and Xiaowei Wang. "A Wideband Divide-by-2/4 Static CML Frequency Divider With Quadrature Outputs." *2024 9th International Conference on Integrated Circuits, Design, and Verification (ICDV)*. IEEE, 2024.

