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Hybrid Protection Of Digital Fir Filters

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Abstract: Digital signal processing makes extensive use of finite impulse response filters. Thanks to a plethora of studies conducted over the last 20 years, the numerous constant multiplication blocks are now much easier to execute. Unfortunately, the structural adders and registers in the taps delay and accumulate line halt any further reduction in space and power consumption. These components make up the majority of the FIR filters hardware cost and are not amenable to current resource sharing strategies for minimizing their impact. The throughput can only be improved by moving or retiming the structural adders and registers. We reframe the filter coefficient synthesis issue to investigate the design space for the tap delay and the accumulation line by cutting it in half at a certain tap point to bridge the area power efficiency gap. We provide a genetic algorithm that efficiently refines the search space to discover an optimum solution that meets the frequency response parameters, solving the integer programming issue at quadratic computational cost. Results from twelve comparison filter specifications using application specific integrated circuit logic synthesis and field programmable gate arrays demonstrated that our suggested algorithm reduced power consumption by 27.5% and average area by 26.8% compared to solutions obtained using current design methods.

Index Terms - FIR filter design, structural adder, digital signal processing.

Introduction

Since it is stable and has a linear phase response, the FINITE IMPULSE RESPONSE(FIR) filter is ideal for signal conditioning in the digital domain. With the smart devices power budgets and footprints being squeezed by technological revolutions like the impending 5g communication and the recent proliferation of augmented and virtual reality multimedia applications, research into low complexity fir filter design methodologies is thriving. One component of the soon to be established Internet of Things (IoT) is the digitization and linking of dispersed nodes and sensors with a centralized computer resource. Integrating diverse sensors into an intelligent sensor network is another need of Industry 4.0 to prove completely automated control. You need the right signal conditioning circuits to filter out unwanted sounds and interferences. Tables through stagnation in the size, power, sensitivity, and accuracy of application specific digital filters will affect the techno-optimism of the Internet of Things and associated technologies. These filters have a significant function in the signal-to-noise ratio (SNR), reaction time, resilience, and mobility of sensor networks. The complexity of the structural adders and registers in the tap delay and accumulate (TDA) block of a low complexity FIR filter is mostly disregarded by existing algorithms that aim to reduce the multiple constant multiplication (MCM) block. The most important factor is that structural adders operands are sourced from several input samples that are time delayed. Resource sharing via the deletion of similar subexpressions is not possible since there is neither exploitable correlation nor apparent redundancy, unlike the MCM block. Regrettably, these structural adders impede further area and power reduction efforts in FIR filter implementation due to their higher cost and power consumption compared to the sharable adders in the optimized MCM block. To improve the filters throughput or decrease its overall complexity, many new algorithms have looked at this issue and changed the construction of the TDA block.

I. PROPOSED SYSTEM

The growing demand for high-performance and reliable signal processing systems necessitates the development of advanced protection mechanisms for digital filters, particularly Finite Impulse Response (FIR) filters. FIR filters are widely used in applications such as communication systems, audio processing, and embedded systems due to their inherent stability and linear phase characteristics. However, as these systems are exposed to various types of faults and disturbances, the need for robust protection methods to ensure their continuous functionality becomes critical. This chapter introduces a hybrid protection system designed to enhance the reliability and fault tolerance of FIR filters by combining traditional protection mechanisms with modern fault-tolerant strategies.

The proposed hybrid protection system aims to address the limitations of conventional protection techniques that often fail to meet the real-time requirements of modern signal processing applications. By incorporating both redundancy techniques and self-handling methods, this system ensures that FIR filters continue to operate even in the presence of errors or hardware malfunctions. The combination of traditional error detection, correction algorithms, and modern approaches like dynamic fault recovery is central to the success of this system. This hybrid approach offers the advantage of adaptability and scalability, making it suitable for a wide range of applications, from embedded systems to more complex communication networks.

This system's design aims to provide a seamless, fault-tolerant operation without compromising the performance of the FIR filter. It leverages intelligent fault detection algorithms that trigger appropriate corrective actions based on the severity of the fault. By doing so, it minimizes the impact of the faults on the system's overall performance, by ensuring it integrity of the processed signals. Ultimately, the proposed system offers a balanced solution between traditional and modern techniques, enhancing the overall robustness and reliability of FIR filters in critical applications where continuous and error-free operation is essential.

II. IMPLEMENTATION

The growing demand for high-performance and reliable signal processing systems necessitates the development of advanced protection mechanisms for digital filters, particularly Finite Impulse Response (FIR) filters. FIR filters are widely used in applications such as communication systems, audio processing, and embedded systems due to their inherent stability and linear phase characteristics. However, as these systems are exposed to various types of faults and disturbances, the need for robust protection methods to ensure their continuous functionality becomes critical.

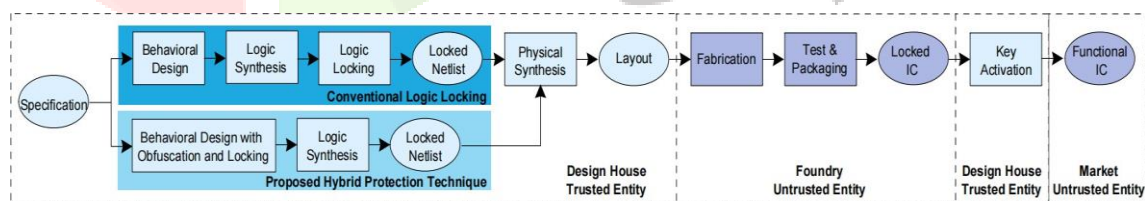


Fig.1 Block Diagram of Proposed Hybrid Protection Technique

The diagram compares Conventional Logic Locking and a Proposed Hybrid Protection Technique in IC design and manufacturing. In conventional logic locking, behavioral design is synthesized into a locked netlist after logic locking, followed by physical synthesis, layout creation, fabrication, testing, and key activation to produce a functional IC. The proposed hybrid approach introduces obfuscation along with logic locking during the behavioral design stage, adding an extra layer of security against reverse engineering. This ensures that the IC design remains secure even before the locking process, enhancing protection against unauthorized use and attacks throughout the IC development lifecycle.

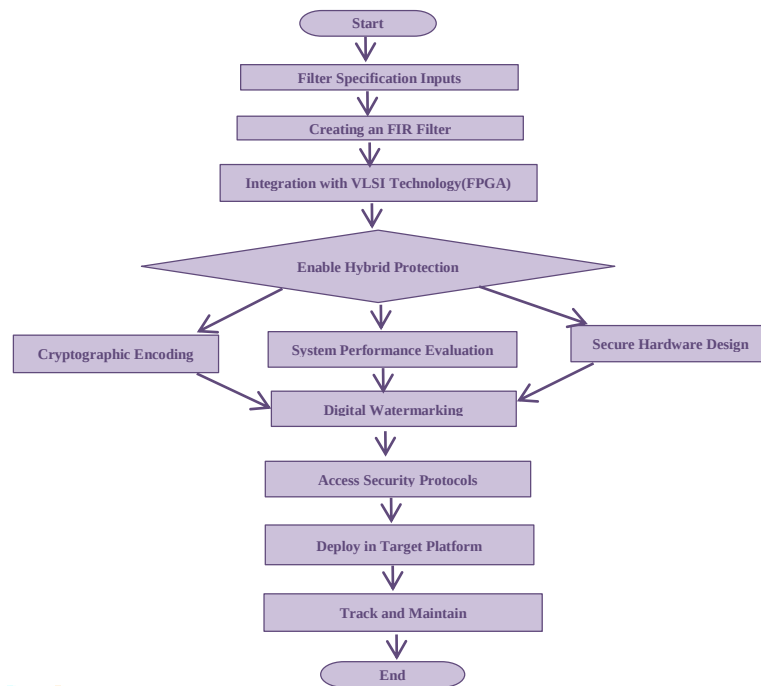


Fig. 2 Flowchart of the digital FIR filter with Hybrid Protection Technique

Complexity of MCM and TDA Blocks in FIR Filter: Using this discrete time convolution, one may create an N-tap digital filter with finite impulse response (FIR).

$$y[n] = h[n] * x[n] = \sum_{i=0}^{N-1} h[i]x[n-i] \quad (1)$$

Where $x[n]$ and $y[n]$ are the n-th time domain input and output samples, respectively. $h[i]$, $i=0,1,\dots,N-1$, are the filter coefficients of the impulse response function.

Table 1: Comparison of Hardware Resources between MCM and TDA blocks

Filters	FIR1 [18]	FIR2 [19]	FIR3 [20]	FIR4 [7]
N	24	37	43	121
w	12	8	16	16
MCM	#FA	129	21	323
	#FS	220	36	226
TDA	#FA	461	528	861
	#FF	459	523	853
TDA/MCM	2.6	18.4	3.1	4.5

P_i is the output of the i-th register R_i of the TDA block and q_i is the i-th coefficient multiplier output $h(i) \cdot x[n]$ of the MCM block in Figure 3. These two variables are the inputs to the i-th SA, which is represented by A_i . The word length of a signal variable α is represented by $w(\alpha)$. By dividing a chosen long partial sum p_j at the j-th tap into two halves, p_{uj} and p_{lj} , as shown in Figure 3, the sizes of some SAs may be decreased (see to [14]). The bottom component p_{lj} may be added to q_i by using decreased word length SAs, A_i for $i = j, j-1, \dots, j \rightarrow m$, while the top part p_{uj} is saved for m ($1 \leq m \leq j$) delays. Where $w p_{j-m-1} > w p_{lj}$, the stored value p_{uj} is added to the signed extended p_{lj-m-1} after $m-1$ cycle delays. If m and j are equal, then the output of the last SA A_0 is represented by $p-1$.

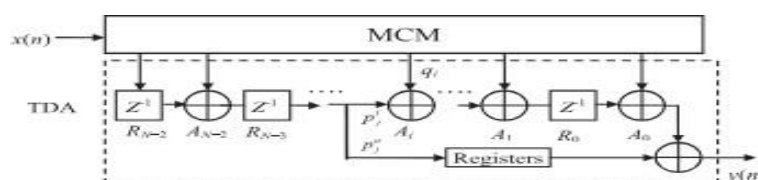


Fig. 3 TDA block with Bisection technique

Here is how interval arithmetic may be used to estimate the bit width $w(A_i)$ of each reduced SA A_i for $i = j, j-1, \dots, j-m$:

$$w(A_i) > \left\lceil \log_2 \left(\max \left(2^{w(p_j^l)} - 1 + \sum_{i=j-m}^j v_i^+ - \sum_{i=j-m}^j v_i^- \right) \right) \right\rceil \quad (2)$$

The dynamic range of q_j is denoted by $v^+ + j$ and $v^- - j$, whereas $\cdot$ is the ceiling function. $W(A_i)$ grows monotonically with i , as long as $v^- - i < 0$ and $v^+ + i > 0$. The total number of FAs saved by the m decreased SAs beginning from the j -th tap is obtained by assuming that the SA implementation uses a ripple carry adder (RCA) to preserve space and power.

$$\Delta_{j,m} = \sum_{i=0}^m \left[w(p_j) - w(A_{j-i}) - \rho (w(A_{j-i}) - w(p_j^t)) \right] - [w(A_{j-m}) - w(p_j^t)] \quad (3)$$

In (2), $w(p_j) - w(A_{j-i})$ represents the FA cost saving and $w(A_{j-i}) - w(p_j^t)$ represents the register overhead required the area ratio of an FA to an FF, in order to preserve p_j form cycles. The FA cost needed to combine the saved p_j is denoted by the final equation, $w(A_{j-m}) - w(p_j^t)$. While $w(p_j^t)$ may take on any value less than $w(p_j)$, we set it equal to $w(q_j)$ in order to reduce the SAs. The amount of delay cycles, which is $m - 1$, before merging, and the tap location j to separate p_j seem to be the variables that determine j, m . The goal is to find out how much of an impact it has on reducing SA costs by doing only one addend split at a given tap position j with $m = j$, such that all SAs from the j -th tap to the output may be minimized, as seen in Figure 3. The values of $j = j, j$ at various splitting positions j for FIR1 to FIR4 with $\rho = 1$ are listed in Table 2.

Table 2: FA Cost & FA saving by Direct Application of TDA Bisection Technique

FIR1 (N=25)			FIR2 (N=37)			FIR3 (N=43)			FIR4 (N=121)		
j	FA	Δ_j	j	FA	Δ_j	j	FA	Δ_j	j	FA	Δ_j
11	920	0	11	1051	0	11	1714	0	11	5145	0
12	1160	-240	22	1355	-304	21	2176	-462	60	6585	-1440
11	1140	-220	20	1351	-300	19	2132	-418	55	6244	-1099
10	1100	-180	18	1339	-288	17	2018	-304	50	6045	-900
9	1064	-144	16	1307	-256	15	1984	-270	45	5955	-810
8	1047	-127	14	1215	-164	13	1918	-204	40	5785	-640
7	1032	-112	12	1195	-144	11	1890	-176	35	5705	-560
6	1011	-91	10	1131	-80	9	1837	-123	30	5565	-420
5	994	-74	8	1097	-46	7	1812	-98	25	5445	-300
4	983	-63	6	1083	-32	5	1774	-60	20	5381	-236
3	968	-48	4	1075	-24	3	1750	-36	15	5291	-146
2	949	-29	2	1057	-6	1	1724	-10	10	5224	-79
1	935	-15	-	-	-	-	-	-	5	5173	-28

III. RESULTS AND ANALYSIS

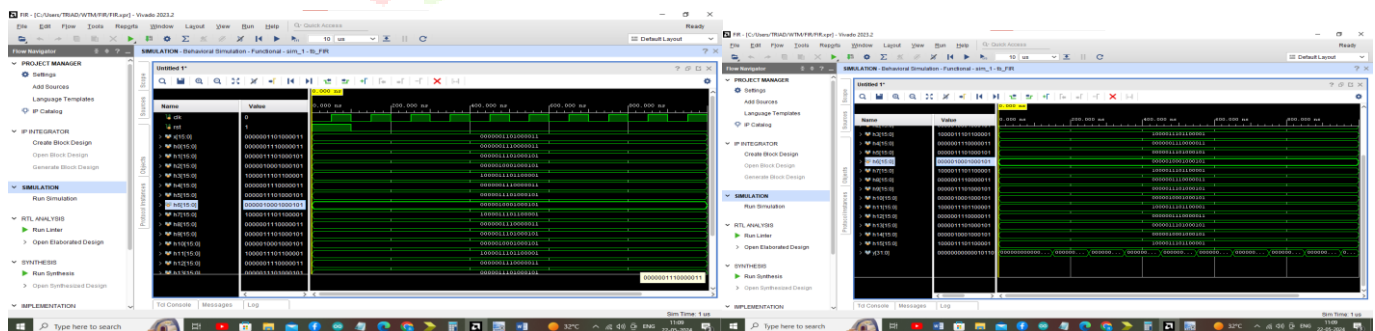


Fig. 4 Simulation waveforms under various test conditions

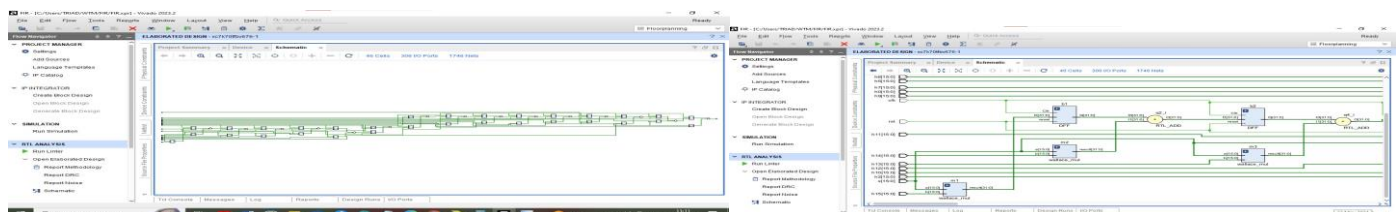


Fig. 5 RTL view of the synthesised design

The results of the project, "Hybrid Protection of Digital FIR Filter," include simulation and synthesis outcomes that validate the system's functionality and design accuracy. The simulation results demonstrate the behavior of the FIR filter, where input signals were applied to observe the corresponding output. These outputs confirm that the filter performs correctly, processing the signals as intended while meeting the defined timing constraints. The waveforms in Fig. 4 depict the accurate response of the filter under various test conditions.

The RTL (Register Transfer Level) view, presented in Fig. 5, provides a graphical representation of the synthesized design. It showcases the internal structure of the FIR filter, including registers, logic gates, and connections. The RTL view ensures that the physical design implementation aligns with the system's architectural and logical requirements, confirming the integrity of the design.

The results highlight the effectiveness of the hybrid protection mechanism in enhancing the reliability of the FIR filter. The protection system ensures that the design can handle faults or errors without compromising the filter's performance. The simulation waveforms further verify the successful detection and handling of such conditions during operation.

VI. ADVANTAGES AND APPLICATIONS

Some of the major advantages related to the implementation of the Hybrid protection FIR filter are that the Hybrid protection mechanisms for FIR filters enhance fault tolerance, signal integrity, and real-time adaptability by combining error detection, correction, and redundancy. These systems reduce maintenance needs, minimize downtime, and offer scalable, cost-effective solutions for diverse applications. Their robustness makes them ideal for critical fields like telecommunications, medical devices, and radar systems. Additionally, they support future-proofing and integration with advanced technologies such as AI and IoT, enabling self-diagnosis, predictive maintenance, and remote monitoring for improved efficiency and reliability.

Hybrid protection-enhanced FIR filters are crucial across a wide range of applications, including telecommunications, audio processing, medical devices, image processing, and radar systems. They ensure reliable, distortion-free signal processing even under challenging conditions like noise, hardware faults, and environmental interference. This robustness is vital in fields such as satellite and wireless communications, control and automotive systems, and data storage, where accuracy and reliability are critical. Additionally, hybrid-protected FIR filters support high-performance operation in navigation, power systems, and aerospace and defense, making them indispensable in both commercial and mission-critical applications.

VII. CONCLUSION

The current design algorithms for FIR filters maximize adder sharing in the MCM block, which fails to adequately reduce the dominating cost of the TDA block. In response, this paper introduces a new methodology for area-power efficient FIR filter implementation that synthesizes the filter coefficients to maximize the savings of the TDA block. Optimal bisection at an ideal tap point reduces the sizes of succeeding structural adders and registers without breaking the filtering standards, and the effective implementation cost of the TDA block is dictated by this. A specialized Genetic Algorithm resolves the issue of regenerated coefficient synthesis. Comparison of synthesis findings in 65nm standard cell technology with designs produced by three different state-of-the-art design algorithms for twelve benchmark filter requirements reveals that our suggested solutions are at least 16.8%.

In this article, the design of a 32-bit multiplier with good performance was realized. The overall power dissipation for the unit is 155.532 mW, and its operating frequency is 215 MHz. Systems requiring high speed from processors executing operations involving a large number of bits may benefit from this architecture, since 32-bit multiplication has a lower latency. The XILINX synthesizer is used to synthesize the Multiplication, and XILINX ISE 12.3 or Vivado 2023.2 is used to verify its operation.

VIII.FUTURE SCOPE:

Emerging trends in hybrid protection for digital FIR filters include the integration of AI, machine learning, quantum computing, and neuromorphic computing to enhance adaptability and fault tolerance. These technologies have potential applications in advanced fields such as 5G/6G communications, IoT, autonomous vehicles, and medical devices. Research is focused on new materials, improved fault tolerance methods, real-time system integration, and cybersecurity. Key challenges include balancing performance with protection, ensuring scalability and flexibility, developing standardization and certification processes, and addressing the need for specialized education and training in this evolving field.

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