



Design Of SAR ADC For Ground Penetrating Radar Application – Literature Review

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Abstract: This paper offers a review of the literature on the theoretical and practical working of SAR ADC for 12-bit resolution and 40-50 MSPS in SCL 180nm technology. Data convertors are essential in any digital processing system. It is instrumental in acquiring sensor data in a meaningful way. In the process of circuit miniaturization, Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) with its simple structure, moderate speed and low power consumption, it is widely used in application fields such as mobile devices, wireless communication, smart sensors, medical imaging and industrial automation. Ground Penetrating Radar (GPR) systems require high-resolution, power-efficient Analog-to-Digital Converters (ADCs) capable of operating reliably in noisy and radiation-prone environments. This literature review examines recent advancements in Successive Approximation Register (SAR) ADCs, highlighting technologies and techniques that address challenges such as resolution accuracy under noise, power-speed-area trade-offs, and the demand for cost-effective, robust designs.

Reference papers were studied, focusing on high-speed, low-power architectures, comparator enhancements, DAC innovations, and layout-level implementations in SCL 180nm technology.

Index Terms - Ground Penetrating Radar (GPR), SAR, C-DAC, Resolution

I. INTRODUCTION

An Analog to Digital Converter (ADC) is a type of device which helps us to process the chaotic real-world data in a digital standpoint. Since the majority of our devices nowadays are digital, it becomes necessary to convert those signals into digital signal and that is where the ADC comes in. An ADC is an essential electronic circuit that transforms a continuously varying analog signal such as temperature, sound, or light intensity into a digital number that can be understood and processed by digital systems like microcontrollers, FPGAs, or computers. Since the real world is analog but most modern processing is digital, ADCs act as a bridge between the two domains. The process of conversion involves three key stages: first, the analog signal is sampled at specific time intervals to capture its amplitude; second, each sampled value is quantized to the nearest available level in a predefined set of digital levels and finally, this quantized level is encoded into a binary number. The quality of this conversion is influenced by parameters such as resolution, sampling rate, accuracy, and power consumption.

GPR systems require robust analog front-end circuitry to digitize reflected electromagnetic signals with high accuracy. The ADC is a critical component of this front-end. Among various ADC architectures, the SAR ADC stands out for its moderate speed, low power consumption, and digital control logic, making it ideal for portable and embedded radar systems. However, when used in GPR applications, SAR ADCs must meet stringent requirements including high resolution in noisy environments, radiation tolerance (especially

for aerospace or underground use), and optimal power, area, and speed efficiency.

II. LITERATURE SURVEY

There are different types of ADCs that exist, each characterized by its unique design trade-offs and advantages:

The Successive Approximation Register (SAR) ADC is one of the most widely used ADC architectures, particularly for applications requiring moderate speed and high resolution. It operates based on a binary search algorithm. The process begins by comparing the analog input to a reference voltage using a digital-to-analog converter (DAC) and a comparator. The SAR logic starts by setting the most significant bit and checks whether the resulting voltage is above or below the input. Based on the comparator's result, it either keeps the bit or clears it and proceeds to the next bit. This process continues until all bits are resolved, typically taking one clock cycle per bit. SAR ADCs are popular in systems like data acquisition units, battery-operated devices, and industrial sensors due to their relatively low power consumption, high resolution (up to 18 bits), and decent sampling speeds (from hundreds of kSPS up to tens of MSPS).

The Flash ADC is the fastest type of ADC architecture and is typically used where extremely high sampling speeds are required, such as in radar systems, oscilloscopes, and RF signal processing. It works by using a large number of comparators in parallel, specifically, for an n -bit ADC, $2^n - 1$ comparators are needed. Each comparator checks whether the input voltage is above a specific reference level, and the set of outputs forms a "thermometer code" that is then encoded into binary. Because all comparisons happen simultaneously, the conversion is extremely fast, often in the giga samples per second (GSPS) range. However, flash ADCs are limited in resolution (usually 4 to 8 bits) because the number of comparators increases exponentially with resolution, leading to high power consumption and large area on silicon. Despite these limitations, flash ADCs are indispensable in applications where speed is the top priority.

Pipeline ADCs strike a balance between the speed of flash ADCs and the resolution of SAR or sigma-delta ADCs. The architecture consists of multiple stages arranged in a pipeline, with each stage resolving a few bits of the input signal. After a stage resolves its bits, it subtracts the corresponding analog voltage (using a DAC) from the input and amplifies the residue before passing it to the next stage. This pipelined operation allows the ADC to convert multiple samples at once—while one stage processes the current sample, another can handle the next. Although this introduces latency of a few cycles, it greatly improves throughput. Pipeline ADCs are typically used in video processing, communications systems, and digital imaging where both speed and resolution (commonly 8–14 bits) are important. They consume moderate power and provide conversion rates in the range of tens to hundreds of MSPS.

Sigma-Delta ADCs are well known for their exceptional resolution and noise performance, particularly at lower sampling rates. The architecture relies on oversampling the input signal at a rate much higher than the Nyquist rate, followed by noise shaping through a feedback loop containing an integrator and a quantizer. The result is a stream of 1-bit data which, after being filtered and decimated by a digital filter, provides a high-resolution output. The key strength of sigma-delta ADCs is their ability to push quantization noise out of the band of interest, making them ideal for applications such as audio recording, biomedical instruments, and other precision measurement systems. However, due to the digital filtering and oversampling requirements, these ADCs tend to have higher latency and are not suitable for high-speed applications.

The Dual Slope ADC is a type of integrating ADC known for its accuracy and noise immunity rather than speed. It works in two phases: during the integration phase, the input voltage is applied to an integrator for a fixed time, allowing the integrator output to ramp up; during the de-integration phase, a reference voltage of opposite polarity is applied and the time it takes to return the integrator output to zero is measured. This time is proportional to the input voltage. Since this architecture averages the input over time, it is inherently immune to noise and power supply fluctuations, making it a good choice for applications like digital multimeters and other slow, precision instruments. However, the method is quite slow and unsuitable for high-speed data acquisition.

Time-based ADCs are relatively modern and operate by converting an analog input into a time interval or frequency, which is then measured digitally. One common approach is to use a Voltage Controlled Oscillator (VCO) where the frequency of oscillation varies with the input voltage. By measuring the number of cycles within a fixed time window or measuring the time taken for a specific number of cycles, the ADC converts the input voltage into a digital code. These ADCs are particularly attractive in advanced CMOS technologies, where scaling of voltage and power is important. They offer potential advantages in terms of integration, power efficiency, and scalability but can suffer from nonlinearity and require careful calibration. They are increasingly being explored in low-power and IoT applications.

Table 1 - comparison of different ADC types

ADC Type	Speed	Resolution	Power	Best For
Flash	Very High	Low	High	RF, Radar
SAR	Medium	High	Low	Data acquisition
Pipeline	High	High	Medium	Imaging, Video
Sigma Delta	Low Medium	Very High	Medium	Audio, Precision
Dual Slope	Very Low	High	Very Low	Multimeters
Time Based	Varies	Varies	Very Low	Advanced CMOS

This review summarizes recent advancements in SAR ADC designs, emphasizing comparator and DAC architectures and evaluates their suitability for a 12-bit, 40 MSPS implementation in SCL 180nm CMOS. SAR ADCs operate on the principle of binary search using a sample-and-hold circuit, a charge redistribution digital-to-analog converter (CDAC), a comparator, and SAR control logic. Each conversion begins by sampling the analog input onto the DAC, followed by N comparison cycles to resolve an N-bit digital output. Their architecture benefits from low power consumption, absence of operational amplifiers, and digital simplicity, which fits well with standard CMOS processes.

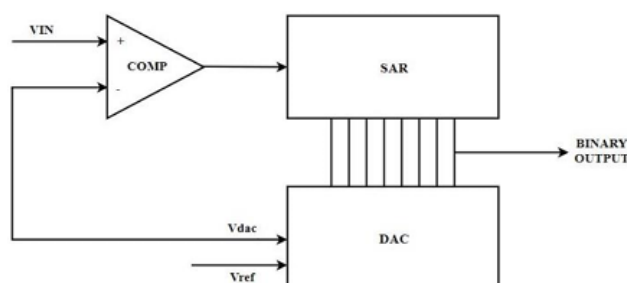


Fig1. Block diagram of SAR ADC

Comparator Design:

The comparator in a SAR ADC is critical because it performs the analog decision-making function during each bit trial. A popular design, the **Strong-Arm latch comparator**, is widely adopted due to its zero static power consumption, high gain, and low offset.

Kishore et al. [8] presented a Strong-Arm latch comparator in 32nm CMOS with a power dissipation of just 1.21 μ W during evaluation, and a propagation delay of 20 ps. Though designed in a more advanced node, its architecture remains valid for scaling to 180nm. Additionally, multiple papers confirm the significance of low-offset, high-speed comparators in SAR ADCs, especially when the resolution exceeds 10 bits. For the 12-bit, a Strong-Arm latch offers an excellent balance between speed and power.

Charge Redistribution DAC and Switching Schemes:

The Digital-to-Analog Converter (DAC) is one of the most critical blocks in a SAR ADC as it directly influences resolution, speed, linearity, and power consumption. Several DAC architectures can be used in SAR ADCs, including capacitor-based DACs (CDACs), resistor-string DACs (RDACs), and current-steering DACs. Among these, CDACs are by far the most commonly used in high-resolution SAR ADCs due to their advantages in area, matching, and energy efficiency. Capacitive DACs (CDACs) function based on charge redistribution, where binary-weighted capacitors are connected and disconnected to a reference voltage during each SAR bit trial. They offer low power consumption, are inherently monotonic, and do not require static current paths—making them ideal for CMOS processes like SCL 180nm. The simplicity and scalability of CDACs also allow for easier layout in deep-submicron nodes, with good linearity if careful matching is done. Moreover, they can be efficiently implemented with Metal-Insulator-Metal (MIM) capacitors which are well-supported in standard CMOS technologies.

In contrast, resistor-string DACs (RDACs) are often used in low-speed applications due to their relatively large area and static power consumption. They require precision-matched resistors and a large number of switches, making layout and temperature tracking more challenging. Because this project on SAR ADC design aims for 12-bit resolution at 40 MSPS in 180nm CMOS, CDAC is the optimal choice. It provides a good trade-off between speed, area, and power. This choice is further validated by the paper from Chung et al. where a CDAC-based SAR ADC using a DAC-configurable window switching scheme was implemented in 180nm CMOS and achieved excellent energy efficiency and dynamic range.

Furthermore, recent advancements such as window switching, VDD-sharing, and monotonic capacitor switching reduce switching energy in CDACs and help in maintaining high linearity. These techniques allow the DAC to avoid unnecessary capacitor transitions, thereby improving both power efficiency and signal integrity.

Successive Approximation Register Logic:

The Successive Approximation Register (SAR) logic is the digital brain of a SAR ADC, responsible for performing the binary search algorithm that determines the digital output corresponding to the sampled analog input. At the beginning of each conversion cycle, the SAR logic sets the most significant bit (MSB) of the digital code to '1' and instructs the DAC to generate the corresponding voltage. This voltage is compared with the input signal by the comparator. Based on the comparator's output—whether the input is higher or lower than the DAC output—the SAR logic decides whether to keep the bit set or clear it to '0'. This process continues bit-by-bit, from MSB to least significant bit (LSB), requiring N clock cycles for an N-bit resolution. The logic stores the result of each comparison and updates the DAC control bits accordingly until the final digital code is fully resolved. Modern SAR logic is implemented using shift registers or finite state machines, often synchronized with a non-overlapping clock to coordinate bit trials precisely. In higher-speed ADCs like yours (40 MSPS), asynchronous SAR logic may also be used to eliminate the need for a high-speed global clock and reduce the critical path delay. In the 12-bit SAR ADC design, the SAR logic must be both accurate and fast, as it governs the full-resolution bit trials within 25 ns (1/40 MSPS). A robust and glitch-free SAR control logic is essential to ensure timing integrity, minimize decision errors, and maintain synchronization

between the DAC switching and comparator evaluation. Since the SAR logic is purely digital, it is highly compatible with SCL 180nm CMOS and offers flexibility for low-power and area-efficient design.

In earlier years, SAR ADCs were mostly associated with low-speed applications such as industrial control systems or digital voltmeters, where moderate resolution and minimal power were more important than speed. They were often overshadowed by faster but more power-hungry architectures like pipeline and flash ADCs in communication or imaging systems. However, with advancements in CMOS technologies, optimization techniques in digital control logic, and innovative analog design (like dynamic comparators and efficient DAC switching), SAR ADCs have undergone a significant transformation. Today, they are capable of achieving speeds in the tens to hundreds of MSPS while maintaining 10–14-bit resolutions—an ideal configuration for radar, biomedical, and IoT-based systems. What makes SAR ADCs particularly important now is their adaptability to modern CMOS processes, such as SCL 180nm technology. They consist of minimal active analog components—primarily a comparator, a capacitive DAC (CDAC), and SAR logic, making them area- and power-efficient. The comparator, once a bottleneck for speed and offset performance, has evolved into compact, high-speed variants like the Strong-Arm latch, which requires no static power and delivers sharp, reliable bit decisions. Similarly, the DAC, historically implemented using resistors or current sources, has transitioned toward charge-redistribution capacitor arrays, which significantly reduce power and support energy-saving switching schemes like monotonic, VDD-sharing, and window-based techniques.

III. CONCLUSION

The design and implementation of a 12-bit, 40 MSPS Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) in SCL 180nm CMOS technology represents a highly efficient and practical solution for Ground Penetrating Radar (GPR) applications. This project has successfully leveraged the strengths of the SAR architecture—digital simplicity, moderate-speed operation, and energy efficiency—to meet the stringent requirements of GPR systems, where high resolution and real-time performance must be balanced with low power and area constraints. A careful selection of key components, including a charge redistribution capacitive DAC (CDAC) and a Strong-Arm latch comparator, ensures that the ADC delivers accurate bit decisions at high speed with minimal power consumption. The CDAC architecture, known for its monotonic response and excellent matching properties, is particularly well suited for 180nm CMOS, providing a compact layout and scalable resolution.

By aligning the ADC's design with recent innovations highlighted in contemporary literature—including window-switching schemes, low-noise comparator topologies, and segmented DAC strategies—this work establishes a strong technological foundation. It also reflects the maturity of SAR ADC design in submicron CMOS technologies and its growing relevance in modern signal-processing systems. Especially in domains like GPR, where precision and efficiency are non-negotiable, the convergence of architectural discipline, process compatibility, and functional adequacy affirms the suitability and future-proof nature of SAR ADCs in radar and beyond.

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