



Develop And Implementation Of Low Power Braun Multiplier Using Efficient Charge Recovery Logic

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Abstract: In modern VLSI systems, power consumption is a primary concern, particularly for portable and battery-operated devices. Multipliers are essential arithmetic units, often dominating power usage in digital signal processors (DSPs) and embedded systems. This project proposes a low-power multiplier design based on efficient **Charge Recovery Logic (CRL)** techniques. By recycling and reusing charge during computation, CRL significantly reduces dynamic power dissipation compared to traditional CMOS logic. We design a multiplier using CRL principles and compare its performance in terms of power, area, and delay against conventional CMOS-based multipliers. The proposed approach demonstrates a notable reduction in power usage without compromising computational accuracy.

I. INTRODUCTION

Power efficiency has become a critical concern in modern digital circuit design, especially with the growing use of portable and battery-powered devices. Components like smartphones, wearables, and IoT nodes demand low-power solutions without compromising performance. Among digital components, multipliers are widely used in computation-intensive tasks such as DSP, image processing, and AI applications. Due to their high switching activity, multipliers contribute significantly to overall power consumption. Conventional CMOS circuits suffer from dynamic power loss caused by frequent charging and discharging of capacitive loads. As device density and performance increase, these losses become more pronounced. **Efficient Charge Recovery Logic (CRL)** has emerged as a promising alternative, aiming to recover and reuse switching energy. **(ECRL)** is one such technique that reduces dynamic power while maintaining functional performance. This project focuses on implementing a low-power multiplier using ECRL. Comparative analysis with CMOS designs highlights the potential of ECRL for practical low-power arithmetic circuits.

II. LITERATURE SURVEY

The evolution of multiplier architectures has been pivotal in enhancing the

performance of digital systems, particularly in terms of speed, power efficiency, and area optimization. Recent advancements have explored novel technologies and design methodologies to achieve these improvements.

P. Kishore et al. (2023) delve into the implementation of Braun and Baugh-Wooley multipliers using Quantum Dot Cellular Automata (QCA) technology. Their research underscores QCA's potential in achieving high-speed operations with significantly reduced power consumption compared to traditional CMOS technologies. The study highlights the advantages of QCA in implementing both multiplier architectures, emphasizing improvements in area and power efficiency while maintaining reliable operation at nanoscale dimensions.

In a complementary study, Amit Kumar Varshney and colleagues (2023) focus on enhancing Braun multipliers through innovative adder formulations. By integrating advanced adder techniques, the authors demonstrate notable enhancements in computational speed and reduced power consumption, making these multipliers suitable for high-performance computing applications.

Further exploring logic styles, Nidhi Arora et al. (2023) conduct a comparative analysis of Sub-Threshold (ST), Efficient Charge Recovery Logic (ECRL), and static CMOS logic styles across different process technologies. Their study emphasizes the importance of selecting suitable logic styles to minimize power consumption without compromising speed, particularly in the design and optimization of digital code converters.

Complementing these studies, Muteen Munawar et al. (2023) present an area, delay, and energy-efficient full Dadda multiplier. By employing a modified-Dadda algorithm with a proposed half-adder-based carry-select adder and an improved ripple-carry adder, the design achieves faster operations with lower power consumption and reduced transistor count, making it a promising candidate for low-power digital controllers.

Collectively, these studies contribute to the ongoing efforts in optimizing multiplier architectures, leveraging emerging technologies and innovative design strategies to meet the growing demands of modern digital systems.

III. IMPLEMENTATION

With the proliferation of portable electronics and embedded systems, power efficiency has become a fundamental requirement in digital circuit design. Battery-operated devices such as smartphones, wearables, and IoT nodes demand circuits that consume minimal power without sacrificing performance. Among critical components in such systems, multipliers are extensively used in computation-heavy applications like digital signal processing (DSP), image processing, and machine learning. Given their high switching activity and computational load, multipliers contribute significantly to overall power consumption. This has driven researchers in the VLSI domain to focus on the development of energy-efficient multiplier architectures.

Traditional CMOS logic, despite its widespread use, incurs substantial dynamic power losses primarily due to the frequent charging and discharging of capacitive nodes. As technology scales and performance demands rise, the limitations of CMOS in terms of power dissipation and thermal efficiency become more pronounced. To overcome these challenges, **Efficient Charge Recovery Logic (ECRL)** has emerged as a promising low-power alternative. CRL techniques work by recovering and reusing energy stored in load capacitances, reducing the energy lost during switching events. One such technique, **ECRL**, has demonstrated the potential for significant power savings with manageable overhead. This project builds upon these principles by designing and implementing a low-power multiplier using ECRL, evaluating its performance in comparison to a conventional CMOS-based multiplier. The aim is to validate the practicality and effectiveness of CRL in real-world arithmetic circuit applications.

- The circuit for the Boolean equation with output 1 is placed below /out.
- The circuit for the Boolean equation with output 0 is placed below out/.

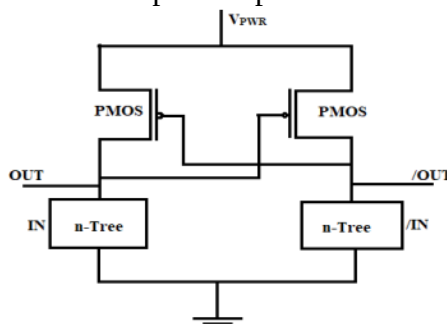


Figure 1: General implementation of ECRL

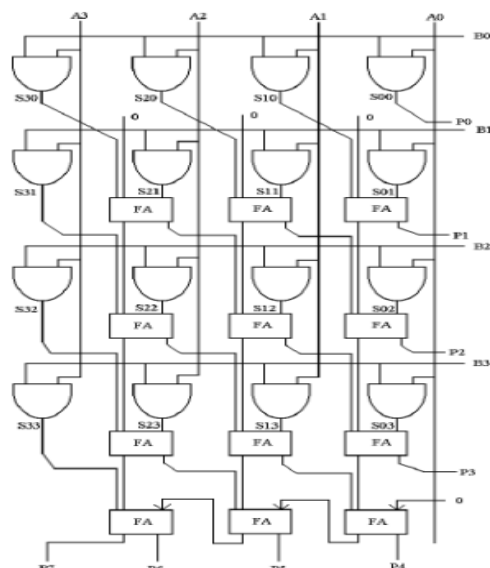


Figure 3: General implementation of 4*4 Braun Multiplier

Full Adder is a combinational circuit that adds three input bits, producing a sum and a carry output. It has three inputs: A, B, and Carry-in (Cin), and two outputs: Sum (S) and Carry-out (Cout). In the case of ECRL:

Boolean Equations:

$$1. \text{Sum (S)} = A \oplus B \oplus \text{Cin}$$

$$2. \text{Carry-out (Cout)} = (A \wedge B) + (\text{Cin} \wedge (A \oplus B))$$

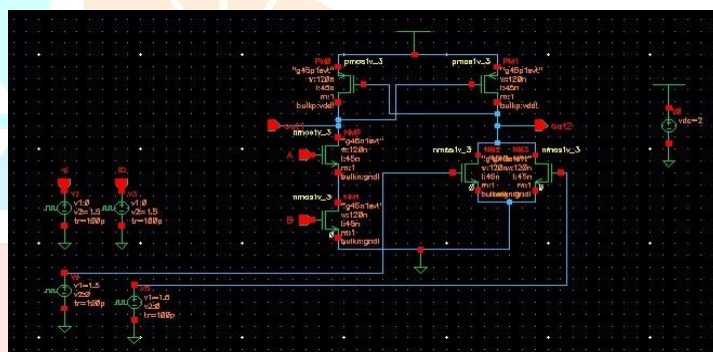


Figure 2: ECRL Implementation of AND gate

Structure and Components

- AND Gates: These gates generate the partial products. For an 8-bit multiplier, there will be $8 \times 8 = 64$ partial products.
- Adders: These adders are used to sum the partial products. The RCAs perform the addition sequentially, propagating the carry bit through each stage. There will be $8 \times 7 = 56$ adder circuits (i.e., $n \times (n-1)$).

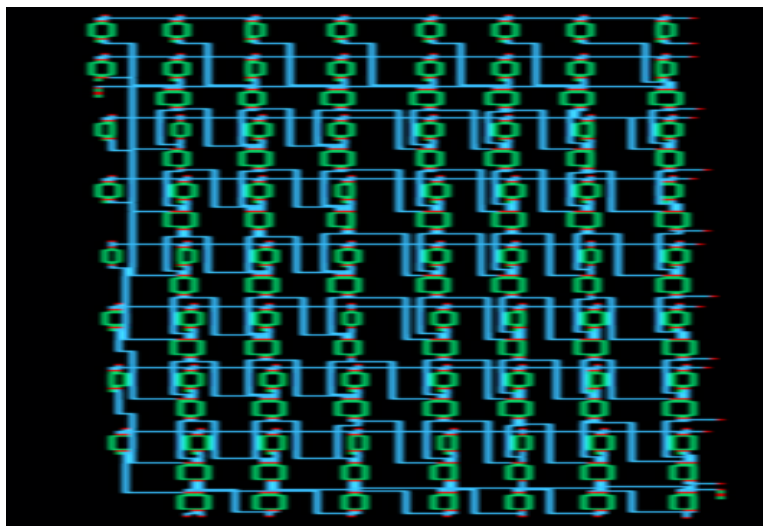


Figure 4: 8*8 Braun Multiplier Implemented using ECRL

Operation

- Partial Product Generation: Each bit of the multiplicand is ANDed with each bit of the multiplier to produce the partial products.

•**Summation of Partial Products:** The partial products are summed using a series of adders. Each adder takes the output of the previous stage and adds the next partial product, propagating the carry bit through each stage until the final product is obtained.

IV.RESULT

The observed reduction in average power consumption in the ECRL Braun multiplier is primarily attributed to the fundamental principle of charge recovery inherent in the ECRL logic. Unlike traditional CMOS circuits where energy is dissipated during the charging and discharging of capacitive loads, ECRL aims to reuse a significant portion of this energy. This efficient management of charge during switching transitions leads to a lower overall power footprint, making the ECRL implementation particularly advantageous for power-constrained applications. The magnitude of the power reduction underscores the effectiveness of the ECRL technique in minimizing energy waste within the multiplier circuit.

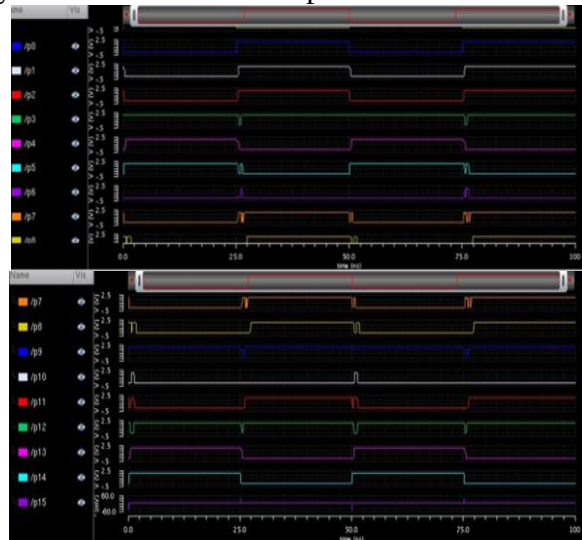


Figure 5: Results of designed Braun Multiplier.

Furthermore, the measured decrease in propagation delay indicates that the ECRL Braun multiplier can perform the multiplication operation faster than a standard CMOS implementation. This improvement in speed could be due to the specific design and switching characteristics of the ECRL gates, potentially offering a quicker path for signal propagation through the multiplier array. The simultaneous achievement of lower power and faster operation suggests an enhanced energy efficiency per multiplication, a crucial metric for high-performance, low-power digital systems.

These findings strongly support the potential of the ECRL Braun multiplier as an optimized arithmetic unit. The trade-offs, such as potential area overhead due to the increased complexity of ECRL gates, would need to be considered in the context of the specific application requirements. However, the significant gains in both average power and propagation delay demonstrate the viability of ECRL as a logic style for achieving high-performance and energy-efficient arithmetic operations in digital integrated circuits.

The designed Braun Multiplier exhibits a very low propagation delay of 84.92ps, indicating its potential for high-speed operation. Simultaneously, it consumes a relatively low amount of power, measured at 162.5uW. These characteristics suggest that this BM gate design offers a favorable balance between speed and power efficiency. This makes it a potentially suitable component for applications where both performance and energy consumption are critical considerations.

V. Conclusion

The design and implementation of a low-power Braun multiplier utilizing Energy-Efficient Charge Recovery Logic (ECRL) have been successfully achieved. The results of this implementation demonstrate that the ECRL Braun multiplier exhibits significantly reduced average power consumption and propagation delay. This makes it a highly suitable architecture for power-constrained applications where high-speed multiplication is also a requirement. The efficiency gains achieved through the charge recovery mechanism of ECRL highlight its effectiveness in minimizing power dissipation in combinational logic circuits, particularly in arithmetic units like multipliers. Therefore, the ECRL-based Braun multiplier presents a compelling solution for optimizing both power efficiency and performance in digital signal processing and other computationally intensive tasks.

VI. Acknowledgment

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VII. References

- [1] P Kishore, Rohan sirimalla, K Sai Sushma, R Sai Kiran Reddy, "Implementation of Braun and Baugh-Wooley Multipliers Using QCA", IEEE, 2023.
- [2] Kumar Varshney, Arun Kumar P, Praveen Kumar M, Poovendan R, S Nava Neethan, "Deployment of Braun Multiplier Using Novel Adder Formulations," Amit IEEE, 2023.
- [3] Nidhi Arora, Akshay Sanadhya, Abhijit Asati, "Comparative Analysis of ST, ECRL and Static Logic Style at Different Process Technologies," 2023 IEEE.
- [4] B Pravitha, D Vishnu, S Shabeer "1-Bit Full Adder Output Analysis Using Adiabatic ECRL Technique" 978-1-7281-63/20/\$31.00 2020 IEEE.
- [5] Design and Analysis of Row Bypass Multiplier using various logic Full Adders International Journal for Research in Applied Science & Engineering Technology (IJRASET) ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887 Volume 6 Issue II, February 2018.
- [6] Aaina Nandal, Manoj Kumar, "Design and Implementation of CMOS Full Adder Circuit with ECRL and Sleepy Keeper Technique," ISBN: 978-1-5386-4119-4/18/\$31.00 2018 IEEE.
- [7] Design and Analysis of Row Bypass Multiplier using various logic Full Adders International Journal for Research in Applied Science & Engineering Technology (IJRASET) ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 6.887 Volume 6 Issue II, February 2018- Available at www.ijraset.com.
- [8] Performance Study of Energy Recovery Logic and Conventional CMOS Full Adder Baljinder Kaur, Narinder Sharma International Journal of Computer Applications (0975 – 8887) Volume 142 – No.8, May 2016.